

REMARKS

Applicants would like to thank the Examiner for the thorough review of the application. Furthermore, Applicants would like to confirm the election of Group I, claims 1-12. By this Amendment, claim 36 is cancelled without prejudice or disclaimer solely in an effort to avoid extra claims fees.

The Office Action objects to the Declaration indicating that it does not include the mailing address of each inventor. However, the Declaration filed on October 15, 2001 is a declaration for use with an Application Data Sheet under 35 C.F.R. 1.76. The application Data Sheet as filed with the application (copy enclosed) does include the City, State and Citizenship information for each inventor. Accordingly, withdrawal of the objection is respectfully requested.

The drawings are objected to for numerous informalities, many of which are overcome by virtue of the attached amendment to Fig. 5 that removes the overlapping text corresponding to step S100 and step S110. Applicants further submit that step S110 is at least mentioned in paragraph 59 and the above amendment to the specification corrects a typographical error in paragraph 68 to include a specific recitation to step S410. Accordingly, all objections to the drawings have been overcome.

The Office Action objects to claims 1-12 and rejects the same due to an apparent misunderstanding of the term "coset." At least based on the attached ITU standard for G.992.1, Applicants respectfully submit the term coset is a well-known and commonly used term in the communications art. In particular, section 7.8.3 of the G.992.1 standard specifically states "in a trellis code modulation system, the expanded constellation is labeled and partitioned into subsets ("cosets") using a technique called mapping by set-partitioning. The 4-dimensional cosets...." At least based on this section, Applicants respectfully submit the term is definite, commonly used and well understood in the art.

Regarding claim 11, Applicants respectfully submit that Fig. 2 clearly illustrates a parity check matrix of the LDPC code having an equal number of branches connecting at least one information bit and at least one parity bit with at least one parity node. In particular, random parity check code 130 is used to derive the parity check matrix "H" 140, and "that each column of the parity check matrix 140 has two 1's, and each row has four 1's, this is analogous to the graphical representation of the parity check code 130." (See paragraph 43).

While comparable arguments can be made for claim 12, to further prosecution, and without conceding to the propriety of the rejection, Applicants have amended claims 11 and 12 to recite that the “parity check matrix of the LDPC code represents an equal number of branches...” and “a parity check matrix represents at least one parity node...,” respectively.

Regarding the rejection of claim 3, and at least with reference to paragraph 26, “BER” stands for bit error rate. More specifically, in rebuttal to the rejection of claim 3, paragraphs 27 and 28 state:

In relation to the second requirement of the code having an equal bit error rate (BER) for the information bits and the parity bits, in conventional LDPC coded systems, LDPC codes are used as simple block codes. In these systems, the parity bits are sent as part of the codeword along with the information bits over the channel. At the receiver, the parity bits are used for decoding an error correction of the information bits. After the decoding process is complete, the parity bits are discarded. As a result, the actual BER of the parity bits is not important. For this reason, conventional LDPC coded systems often use codes that have a different BER on the parity bits and the information bits.

According to an exemplary embodiment of this invention, the encoded bits, i.e., the information and parity bits, are used to designate the constellation coset. Therefore, it is important that all of the encoded bits have an equal BER because both the parity and the information bits are used to determine which coset is to be used for decoding. In particular, the LDPC codes are constructed with equal BER on the information bits and the parity bits at least by insuring the LDPC parity check matrix has the same number of branches connecting the information bits and the parity bits with the parity nodes, and the parity nodes are connected to an equal number of information bits and parity bits.

Accordingly, Applicants respectfully submit that claim 3 is fully in compliance with 35 U.S.C. § 112. Applicants further submit the amendments to claim 11 and 12 overcome the rejections under 35 U.S.C. § 112.

The Office Action rejects the claims under 35 U.S.C. § 102(e) as anticipated by and obvious in view of U.S. Patent No. 6,553,535 to Haruhiko (hereinafter “Haruhiko”).

Claim 1 recites, *inter alia*, FEC coding a subset of the data bit signals using an LDPC code to produce FEC coded bit signals, modulating the data bit signals and the FEC coded bit

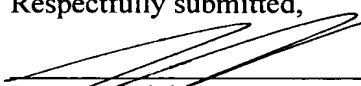
signals using at least one constellation that contains more than one bit signal and designating a coset of the at least one constellation using the FEC coded bit signals.

At no point does Haruhiko teach or suggest the steps as claimed. Applicants nevertheless request the Examiner to contact Applicants' representative to arrange for a Personal Interview should the designating of a coset be unclear or to further discuss the reference's failure to teach the coding, modulating and designating as claimed.

With all objections and rejections having been overcome, Applicants respectfully submit the application is in condition for allowance. An early Notice of Allowance is respectfully solicited.

Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is encouraged to contact Applicants' undersigned representative at the telephone number listed below.

Respectfully submitted,


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